What is claimed is:

1. A testing architecture for automatic test equipment, comprising:

a signal source; and

a plurality of source/capture channels, said signal source coupled to at least one of said channels for providing a signal cancellation signal for reducing an amplitude of a signal received by said channel.

2. The architecture of claim 1 wherein said signal source comprises a Digital-to-Analog Converter (DAC).

3. The architecture of claim 1 wherein said system further comprises an external adjustment device coupled between said source and said plurality of source/capture channels.

4. The architecture of claim 1 wherein at least one of said at least one source/capture channels comprises a capture Analog-to-Digital Converter (ADC) capable of receiving a signal from a device under test.

5. The architecture of claim 4 wherein at least one of said at least one source/capture channels further comprises a combiner receiving a cancellation signal from said signal source, receiving a signal under test, and providing a residual signal from said cancellation signal and said signal under test to said ADC.

6. The architecture of claim 4 wherein at least one of said at least one source/capture channels further comprises:

a combiner receiving a cancellation signal from said signal source, receiving a signal under test, and providing an output signal from said cancellation signal and said signal under test; and

an amplifier receiving said output signal from said combiner and providing an output to said ADC.

7. The architecture of claim 4 wherein at least one of said at least one source/capture channels further comprises:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal; and

a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal to said ADC.

8. The architecture of claim 1 wherein at least one of said at least one source/capture channels comprises:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to said ADC.

9. The architecture of claim 4 wherein at least one of said at least one source/capture channels further comprises an amplifier receiving a signal from said signal source and providing an output to a device under test.

10. The architecture of claim 4 wherein at least one of said at least one source/capture channels further comprises a Digital-to-Analog (DAC) providing an output to a device under test.

11. The architecture of claim 1 wherein said architecture is operable in a first mode wherein each channel is configured to perform a multiple capture, each channel comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to said ADC.

12. The architecture of claim 1 wherein said device is operable in a second mode wherein one channel of said plurality of channels is configured to perform a capture with signal cancellation, said channel comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to said ADC.

13. The architecture of claim 1 wherein said architecture is operable in a third mode wherein each channel of said plurality of channels is configured to perform a capture with signal cancellation, each channel comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to said ADC.

14. The architecture of claim 12 wherein said second mode further comprises the remaining channels of said plurality of channels configured to perform a multiple capture, each of said remaining channels comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to said ADC.

15. A reconfigurable testing architecture for automatic test equipment, comprising:

a signal source; and

a plurality of channels wherein said channels are each configurable into a plurality of modes, each of said modes providing a different level of precision from another of said modes.

16. The architecture of claim 15 wherein said plurality of modes includes a first mode wherein each channel is configured to perform a multiple capture, each channel comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to an ADC.

17. The architecture of claim 15 wherein said plurality of modes includes a second mode wherein one channel of said plurality of channels is configured to perform a capture with signal cancellation, said channel comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to an ADC.

18. The architecture of claim 15 wherein said plurality of modes includes a third mode wherein each channel of said plurality of channels is configured to perform a capture with signal cancellation, each channel comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving a cancellation signal from said signal source, receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to an ADC.

19. The architecture of claim 17 wherein said second mode further comprises the remaining channels of said plurality of channels configured to perform a multiple capture, each of said remaining channels comprising:

a first combiner receiving a signal under test and a baseline signal, and providing a first combiner output signal;

a second combiner receiving said first combiner output signal and providing a second combiner output signal; and

an amplifier receiving said second combiner output signal and providing a residual signal to an ADC.